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NASA TECHNICAL MEMORANDUM

NASA TM-78194

THE MSFC SILICON GATE SILICON-ON-SAPPHIRE STANDARD CELL LIBRARY

By Design Techniques Branch
Electronics Development Division
Electronics and Control Laboratory

September 1978



*George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama*



TECHNICAL REPORT STANDARD TITLE PAGE

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16. ABSTRACT This document is a pictorial representation of the MSFC Silicon-On-Sapphire Standard Cell Library. The cells are intended to be used with the PR2D (Place, Route in 2 Dimensions) Automatic Layout Computer Program.					
17. KEY WORDS					
19. SECURITY CLASSIF. (of this report) Unclassified			20. SECURITY Un		

THE
MSFC SILICON GATE
SILICON ON SAPPHIRE
STANDARD CELL LIBRARY
(with wire bond)

This is a pictorial representation of the MSFC silicon gate, silicon on sapphire standard cell library (for wire bond) revision B dated July 22, 1974. The cells are intended for use with the PR2D program. They were designed by RCA or MSFC as indicated in the cell listing below. Each major grid line represents 1 mil on the chip, minor grid lines represent 0.5, 0.2, or 0.1 mil. One major grid line pair extends beyond the frame, thus pinpointing the location of the cell reference point. Each cell is identified by the technology code "N" and its cell number. The level is indicated below each frame. If no geometry is required on a particular level, the level picture is not shown (dummy levels). Some cells require identical geometries on two or more levels. In this case the geometry is shown only once. The cell listing denotes such duplicate levels.

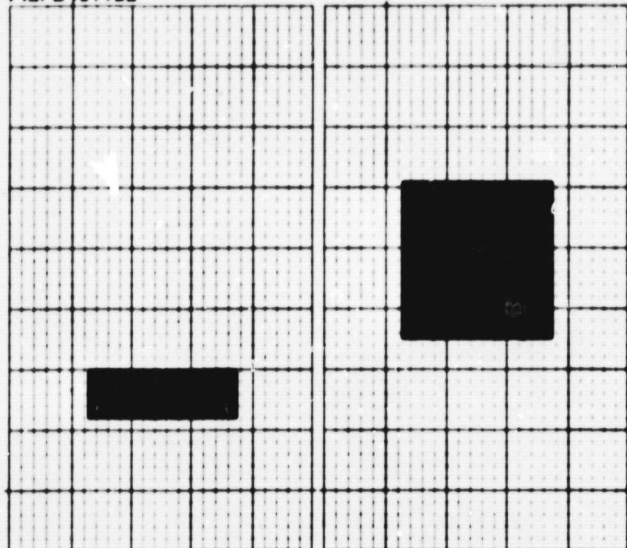
CELL LISTING

CELL #		DUMMY LEVEL(S)	DUPLICATE LEVEL(S)	SOURCE
1120	2 - Input NOR gate	7	-	RCA
1130	3 - Input NOR gate	7	-	RCA
1140	4 - Input NOR gate	7	-	RCA
1220	2 - Input NAND gate	7	-	RCA
1230	3 - Input NAND gate	7	-	RCA
1240	4 - Input NAND gate	7	-	RCA
1310	Inverter	7	-	RCA
1330	$x = B \cdot A + \bar{B} \cdot C$	7	-	RCA
1340	$x = B \cdot A + \bar{B} \cdot C$	7	-	RCA
1510	Non-Inverter Buffer	7	-	RCA
1520	Buffer Inverter	7	-	RCA
1620	2 - Input AND gate	7	-	RCA
1630	3 - Input AND gate	7	-	RCA
1640	4 - Input AND gate	7	-	RCA
1720	2 - Input OR gate	7	-	RCA
1800	3 x 2 - Input AND - 3 X NOR gate	7	-	RCA
1910	$x = \overline{A \cdot B + B \cdot C + C \cdot D}$	7	-	RCA
1920	$x = A \cdot B \cdot C; Y = \overline{B \cdot C}$	7	-	RCA
2310	2 - Input exclusive OR gate	7	-	RCA
2820	D-Master - Slave flip flop	7	-	RCA

CELL LISTING (Continued)

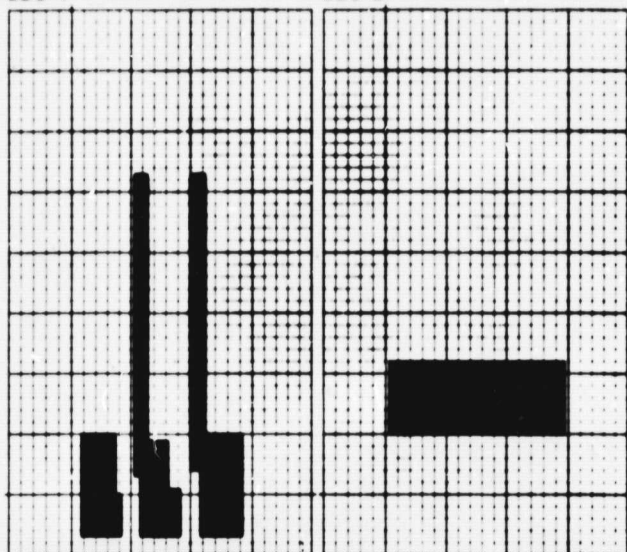
CELL #	FUNCTION	DUMMY LEVEL(S)	DUPLICATE LEVEL(S)	SOURCE
9010	Input Pad	2	-	RCA
9060	VDD Buffer Inverter Pad	-	7=level 7 of cell 9010	RCA
9070	GND Buffer Inverter Pad	-	7=level 7 of cell 9010	RCA
9100	Ground Pad	2, 3, 4, 5	7=level 7 of cell 9010	RCA
9110	VDD Pad	2, 3, 4, 5	7=level 7 of cell 9010	RCA
9210	On-chip alignment mark	-	-	RCA
9220	On-chip alignment mark	-	-	RCA
9250	Off-chip alignment mark	-	2=4=5=7=lev. 1; 6=lev. 3	RCA
9260	Off-chip alignment mark	-	2=4=5=7=lev. 1; 6=lev. 3	MSFC
9310	P - Test Transistor	1, 4	-	RCA
9320	N - Test Transistor	-	-	RCA
9400	Level Identification	-	-	MSFC
9410	Identification "NASA N"	-	2=3=4=5=6=7=lev. 1	MSFC
9420	Identification "MSFC N" (all levels)	-	2=3=4=5=6=7=lev. 1	MSFC
9430	Identification "MSFC N" (lev. 6 only)	1, 2, 3, 4, 5, 7	6=lev 1 of cell 9420	MSFC
9440	Identification "N" (lev. 6 only)	1, 2, 3, 4, 5, 7	-	MSFC
9450	Identification "MSFC" (lev. 6 only)	1, 2, 3, 4, 5, 7	-	MSFC
9500	Feedthrough	1, 2, 4, 7	-	RCA
9700	Numeric Characters 0-9 (all levels)	-	2=3=4=5=6=7=lev. 1	RCA
To				
9790				
9800	Numeric Characters 0-9 (lev. 6 only)	1, 2, 3, 4, 5, 7	6=level 1 of Cell Group 9700/9790	MSFC
To				
9890				

MSFC N1120



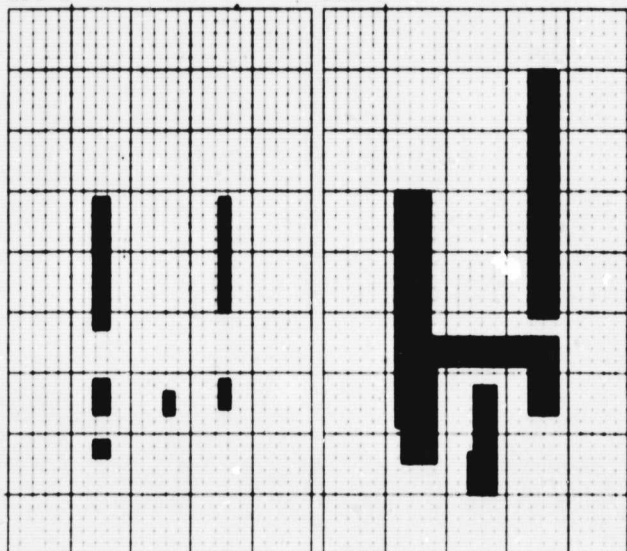
LEV 1

LEV 2



LEV 3

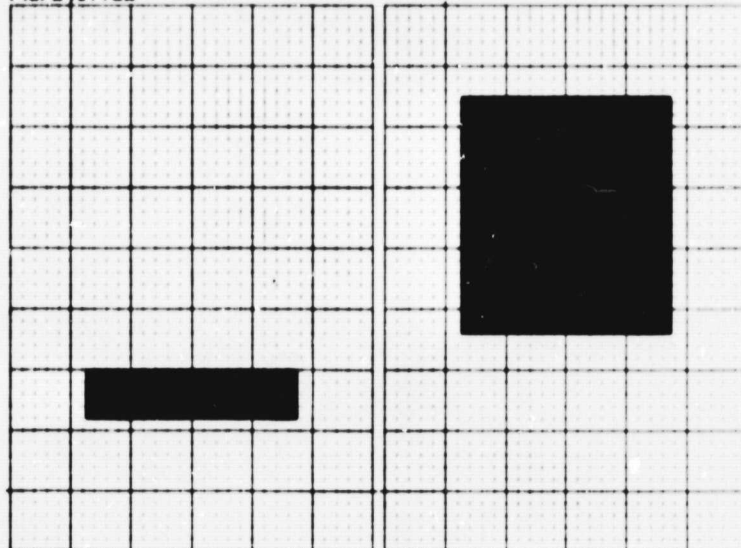
LEV 4



LEV 5

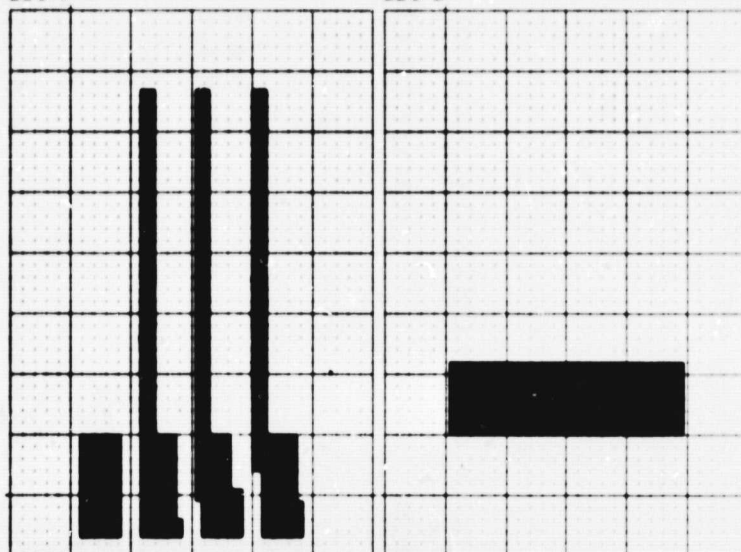
LEV 6

MSFC N1130



LEV 1

LEV 2



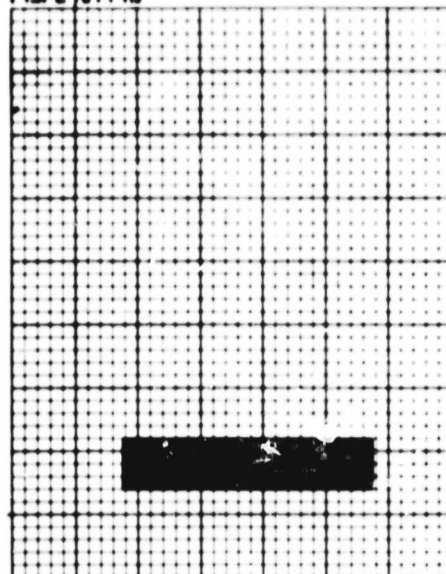
LEV 3

LEV 4



LEV 5

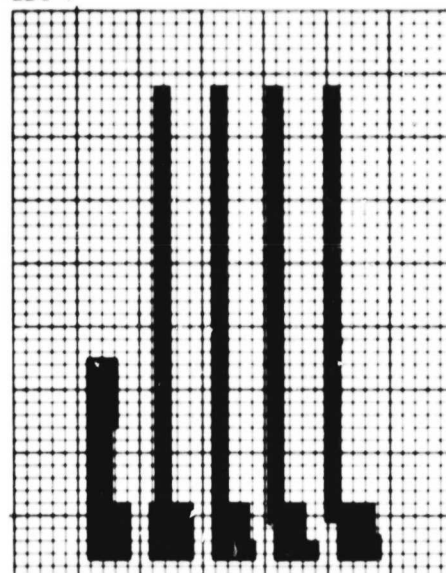
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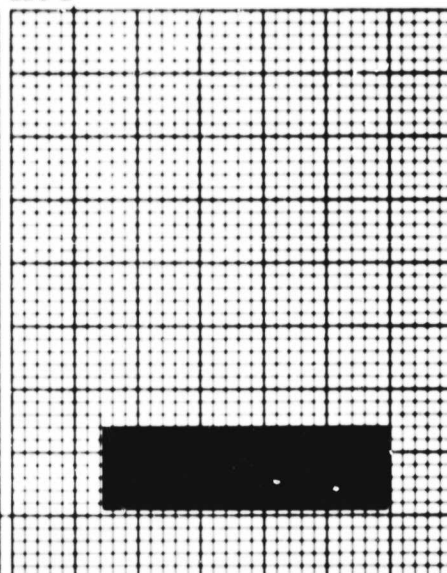
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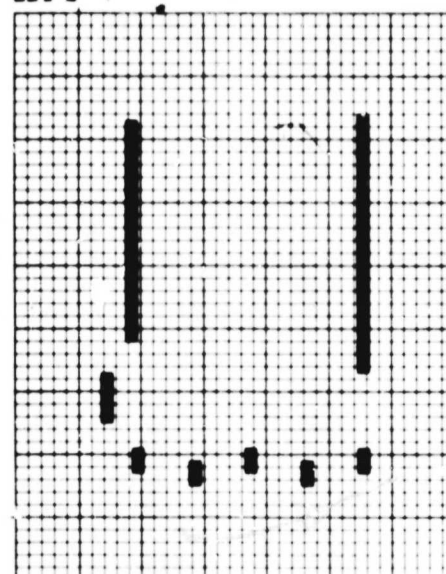
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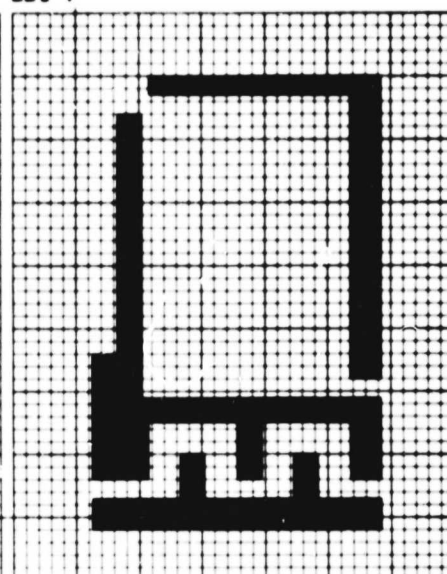
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LEV 4

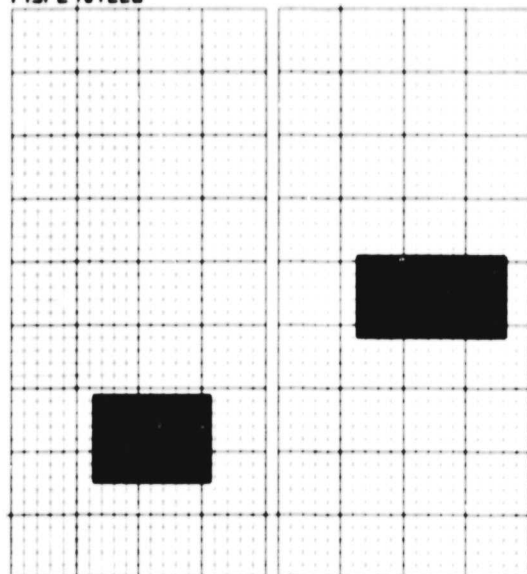


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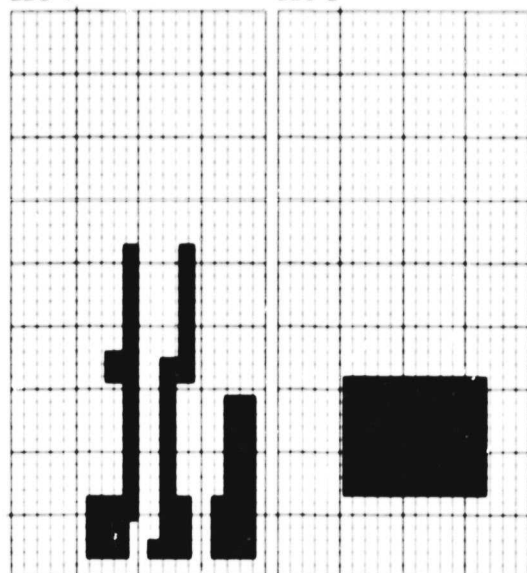
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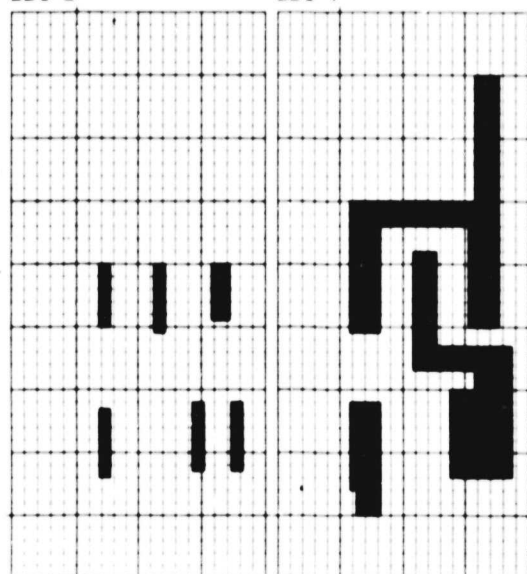
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LEV 2



LEV 3

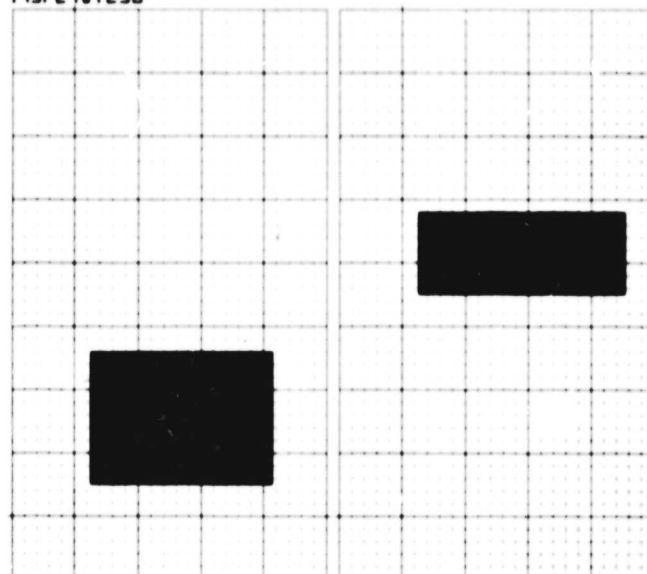
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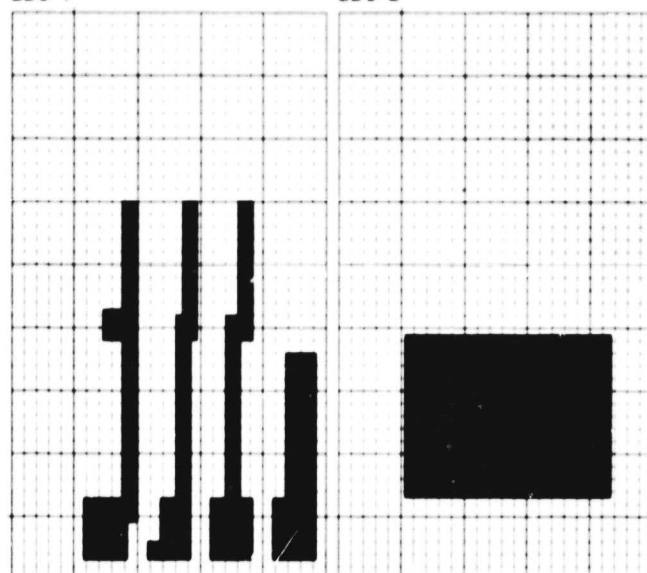
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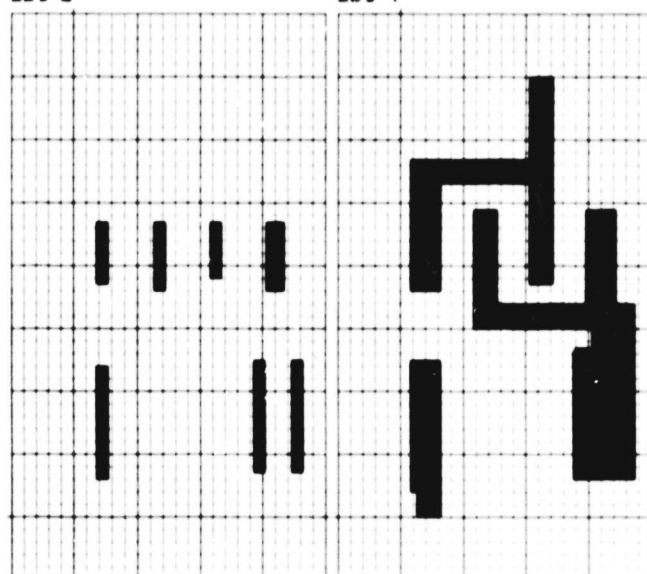
LEV 1

LEV 2



LEV 3

LEV 4

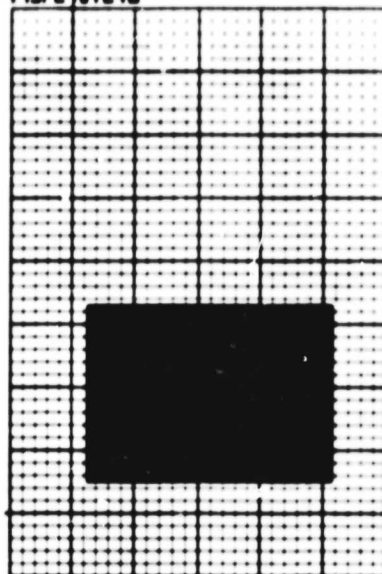


6 LEV 5

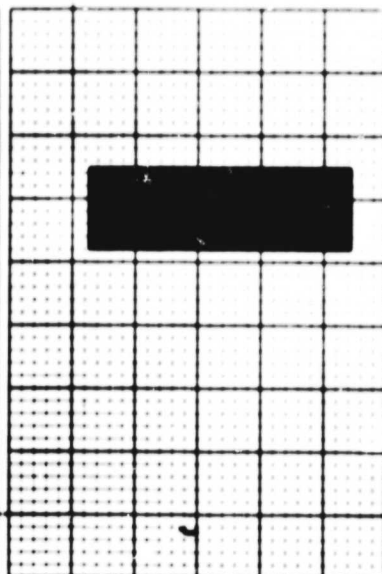
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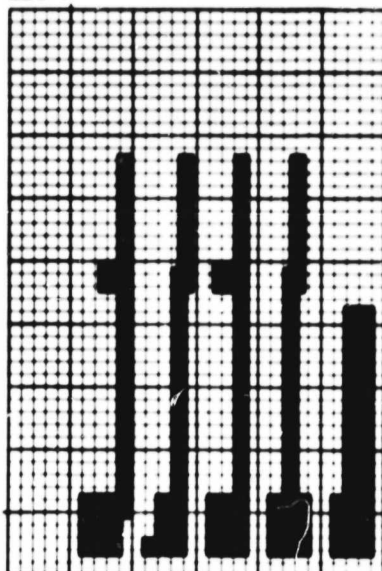
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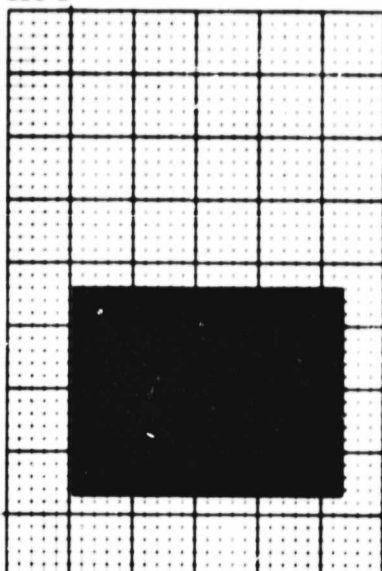
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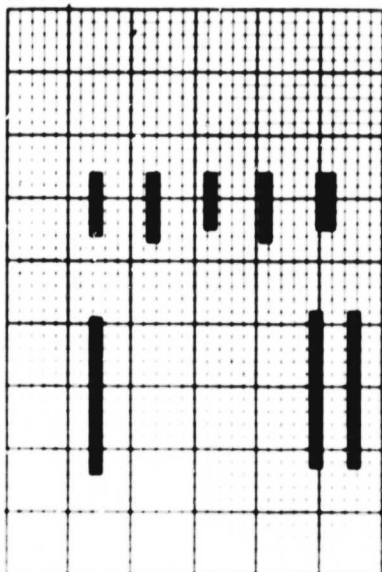
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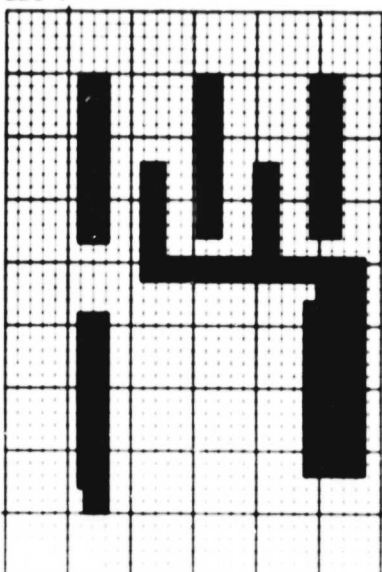
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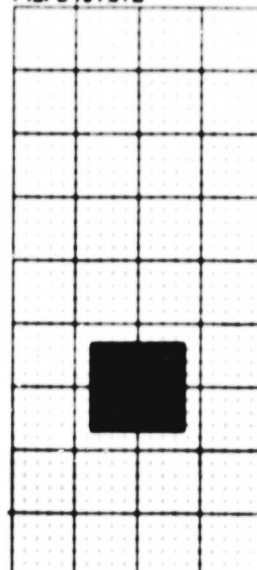


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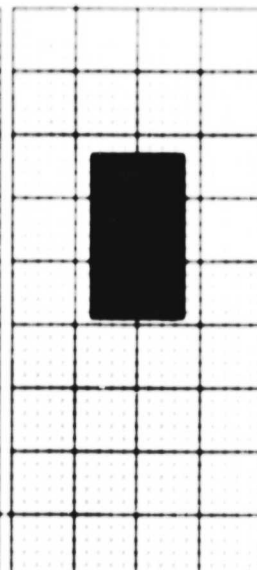


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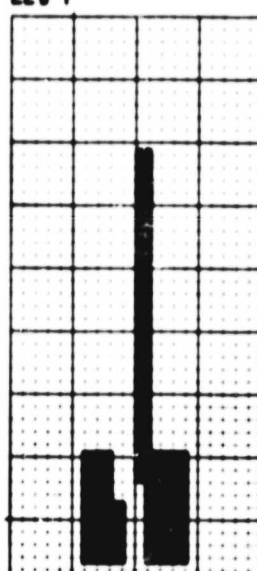
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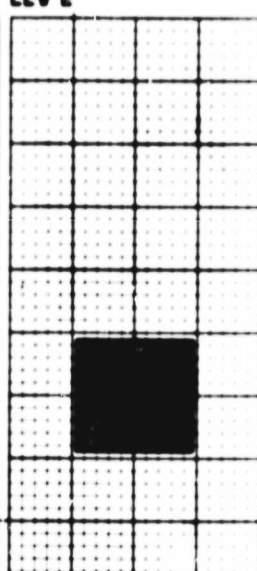
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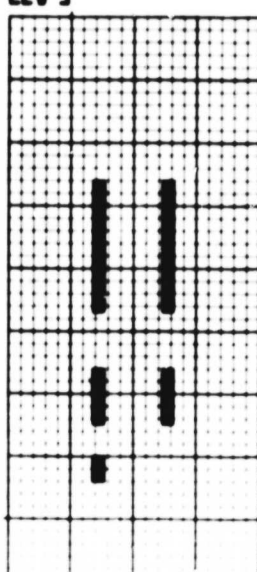
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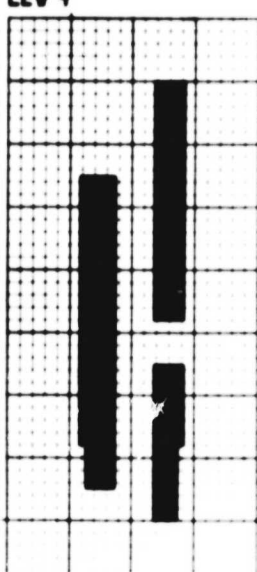
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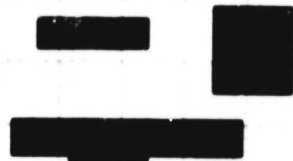
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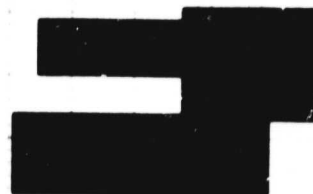
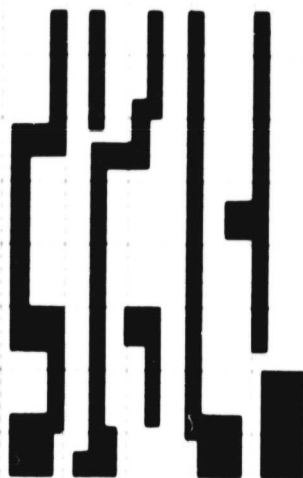


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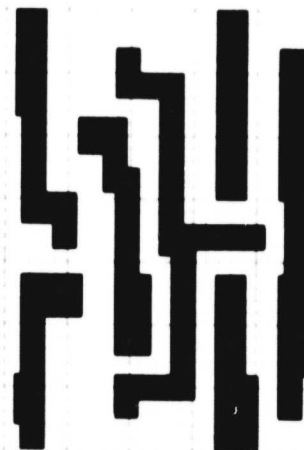
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LEV 2



LEV 3

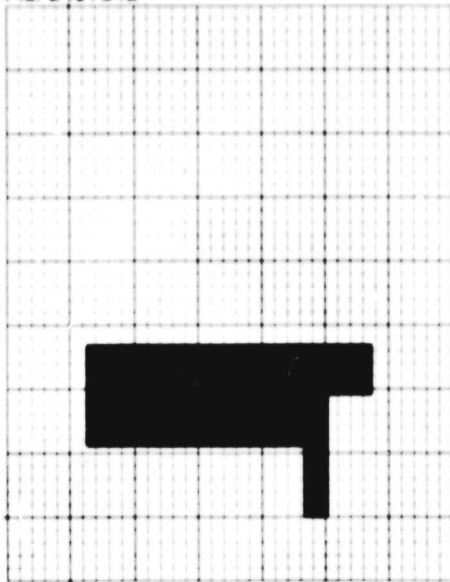
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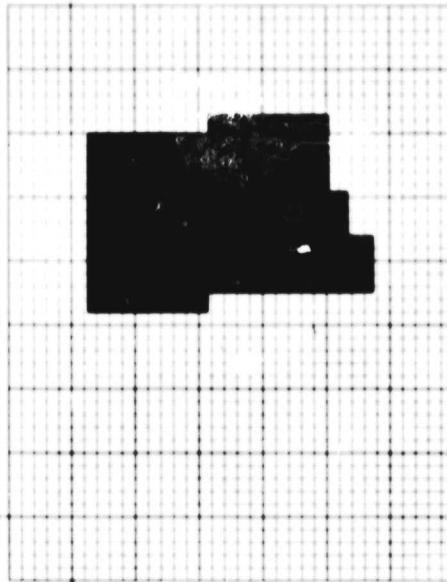
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LEV 6

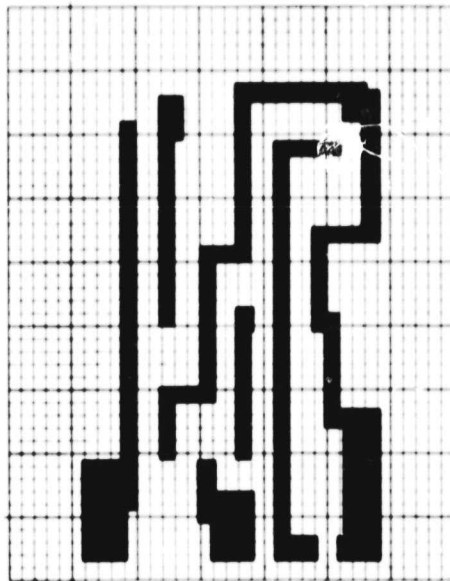
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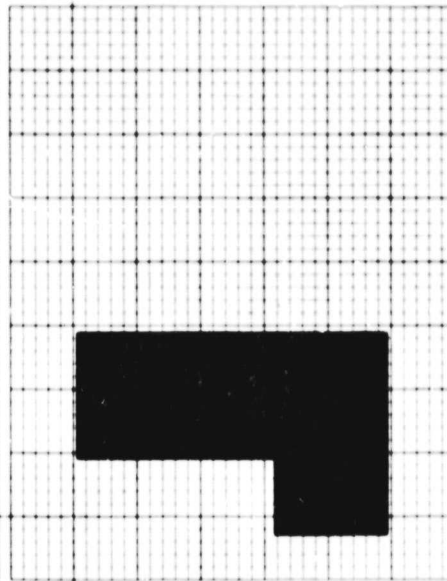
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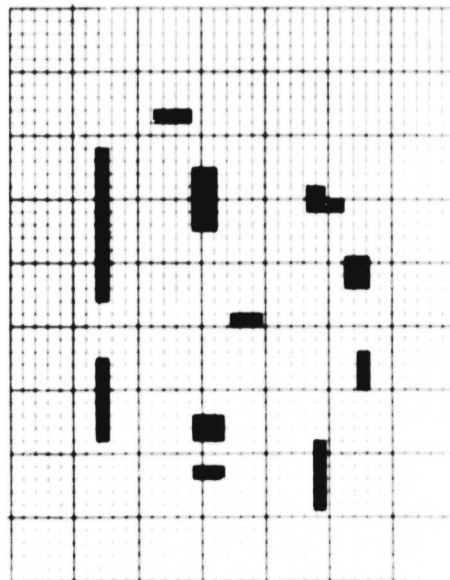
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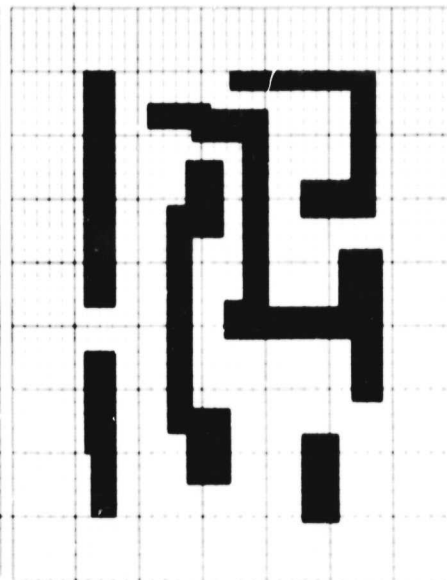
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LEV 4

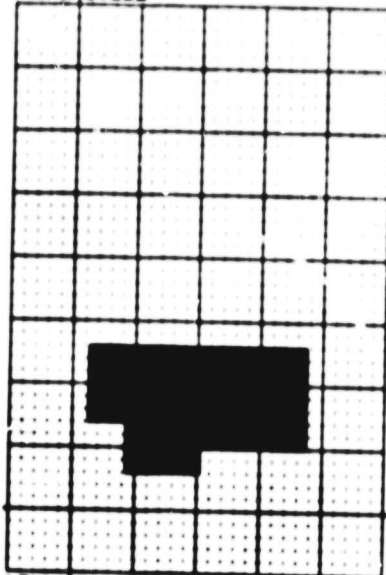


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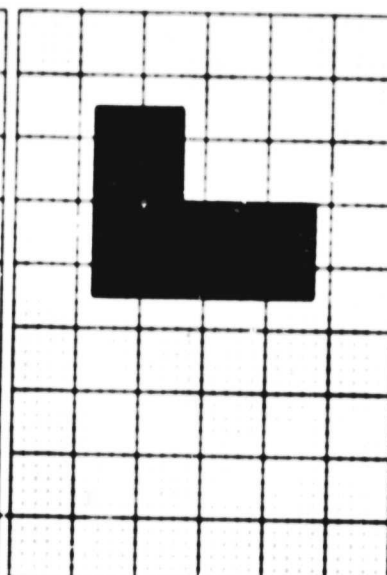


9 LEV 6

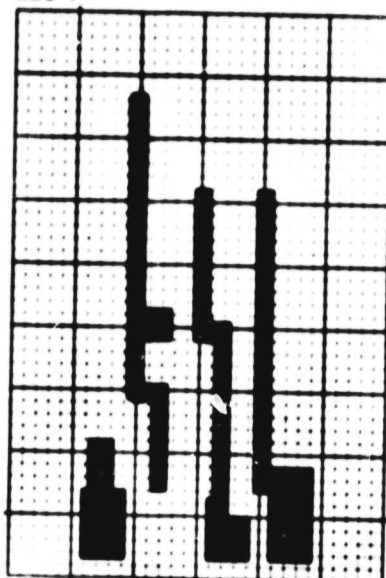
MSFC N1620



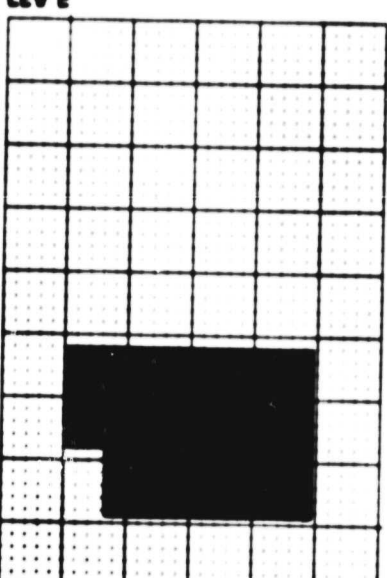
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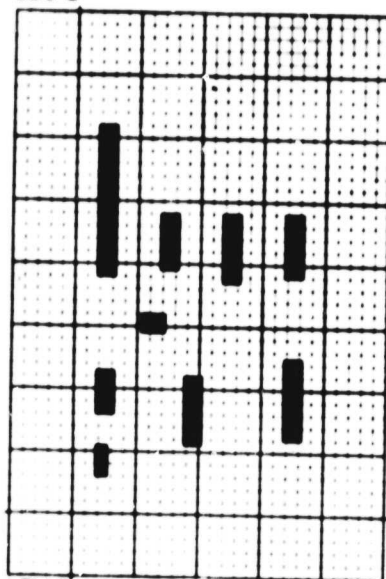
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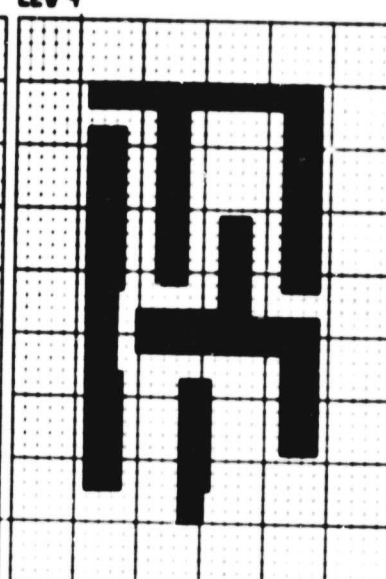
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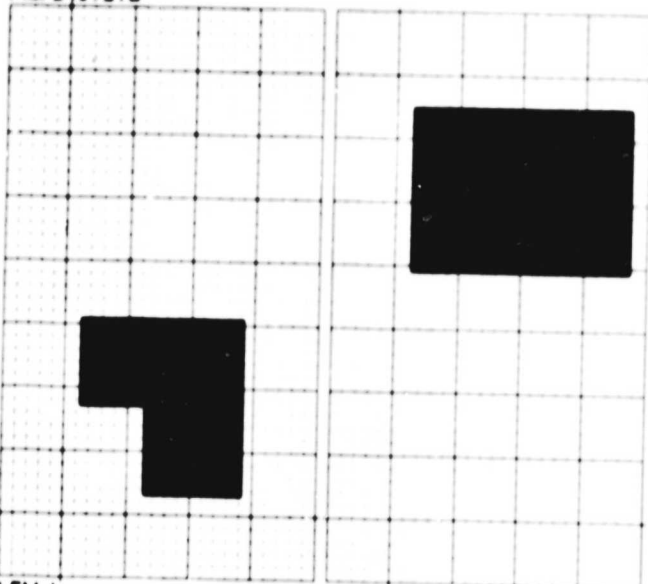


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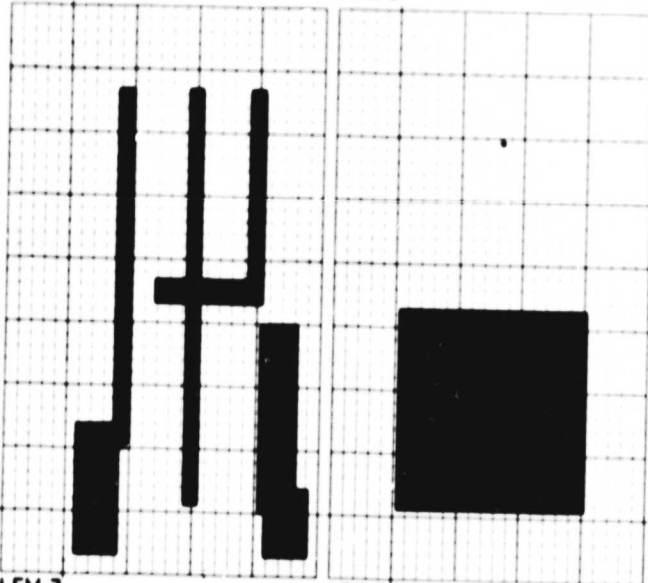
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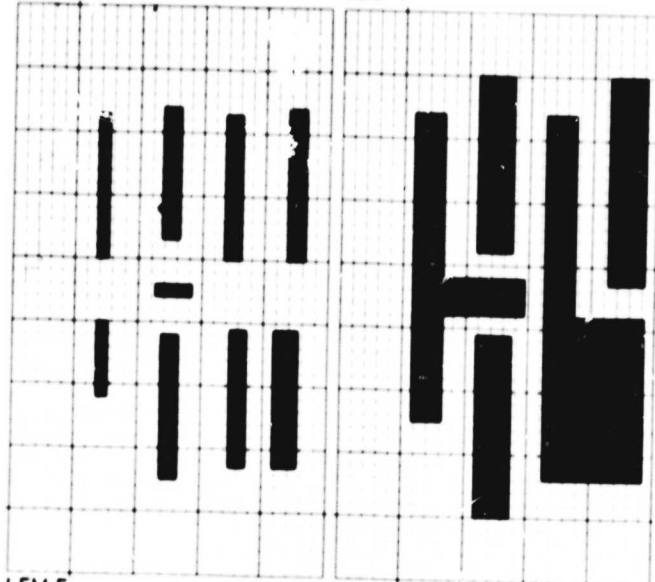
LEV 1

LEV 2



LEV 3

LEV 4

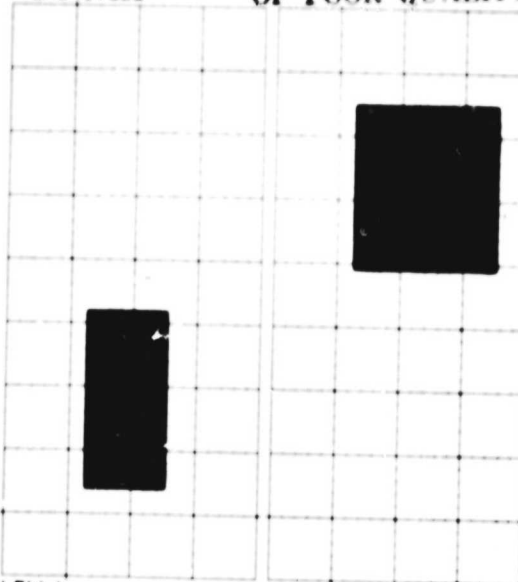


LEV 5

LEV 6

MSFC N1520

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LEV 1

LEV 2



LEV 3

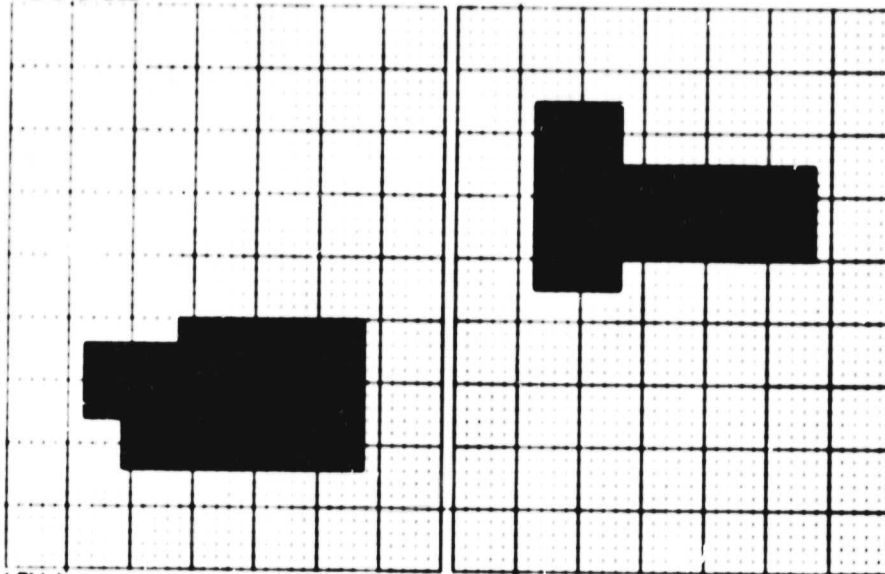
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LEV 5

LEV 6

MSFC N1630



LEV 1

LEV 2



LEV 3

LEV 4

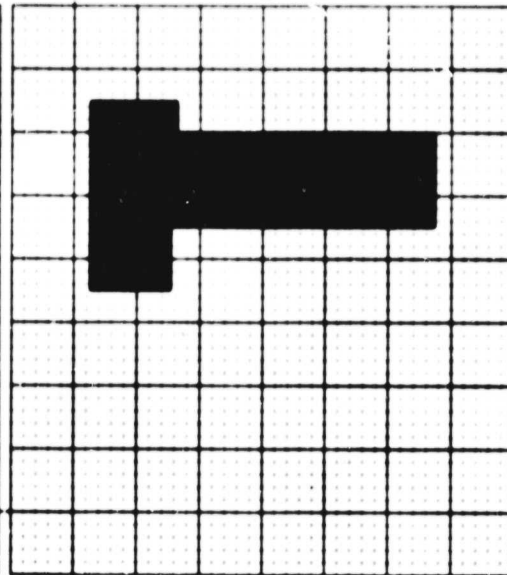
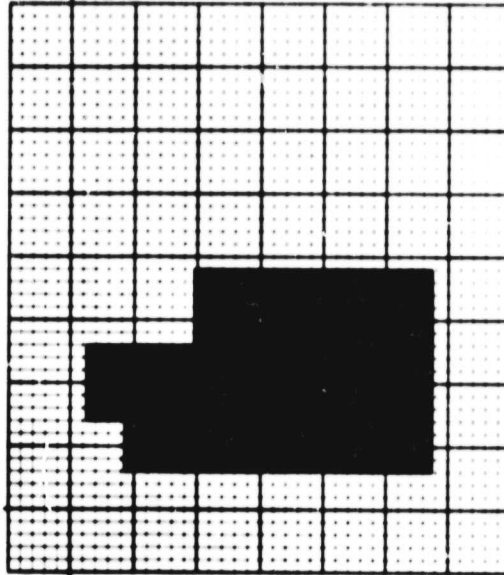


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12 LEV 6

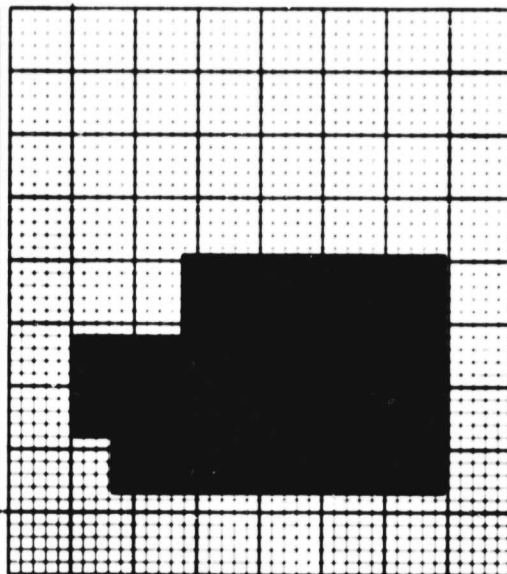
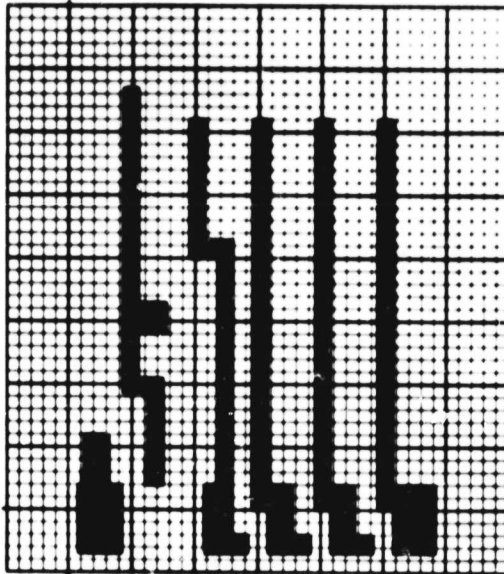
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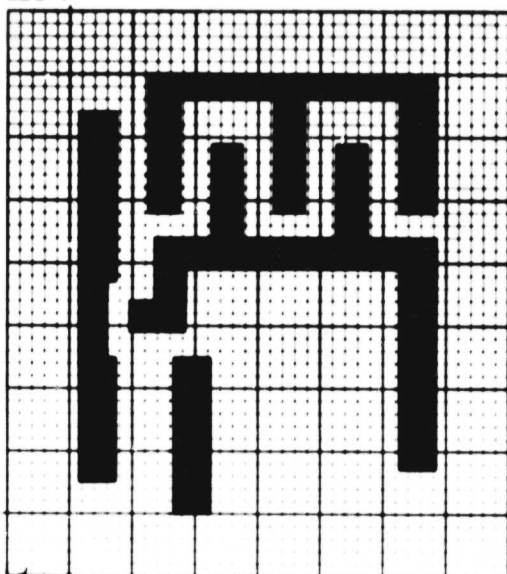
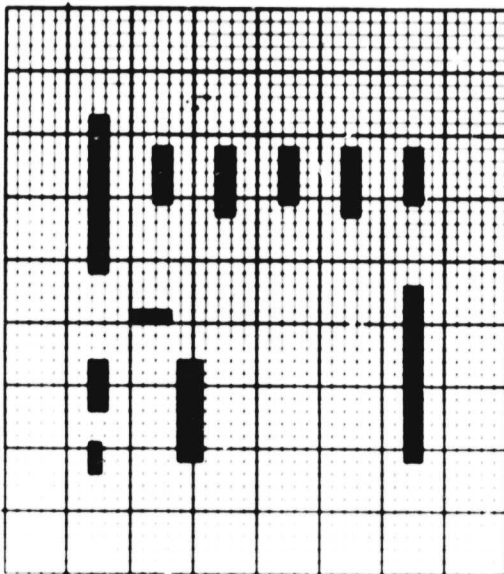
LEV 1

LEV 2



LEV 3

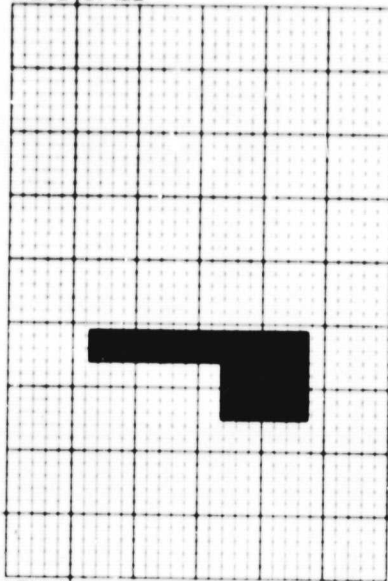
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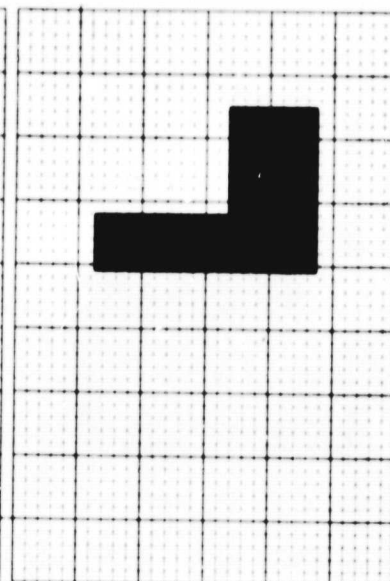
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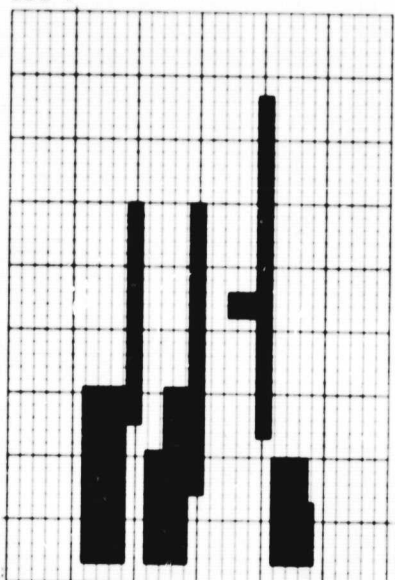
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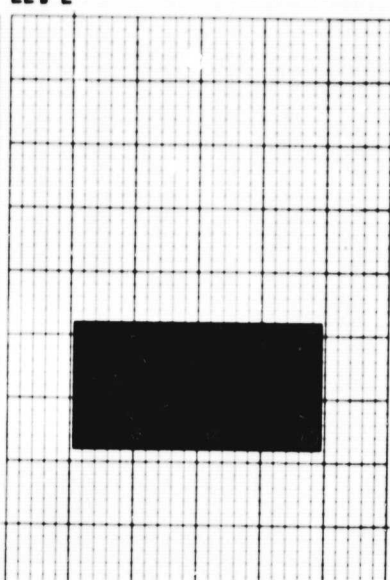
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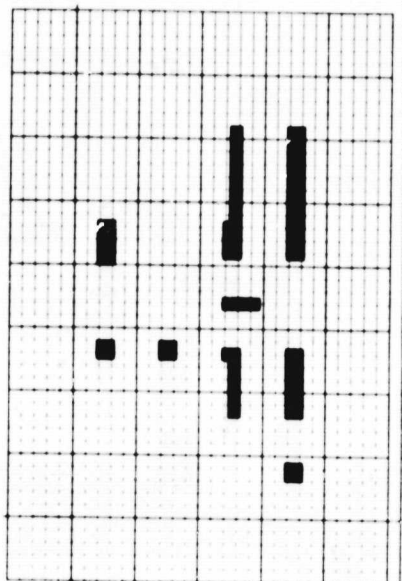
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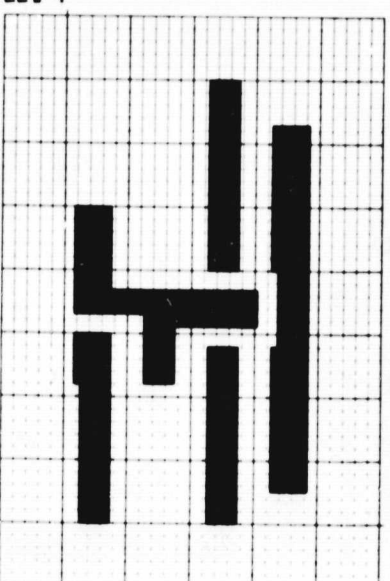
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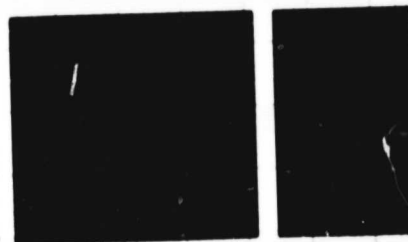
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LEV 5



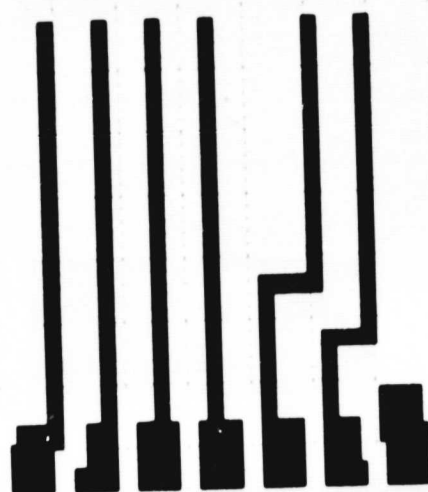
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LEV 1

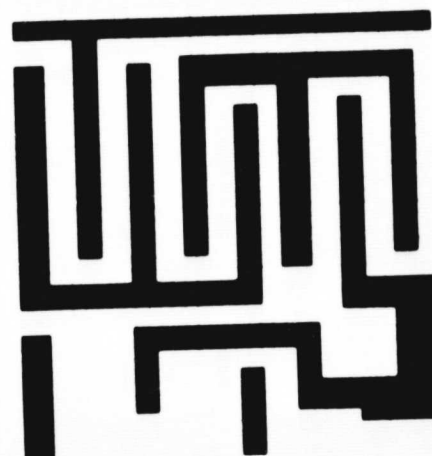
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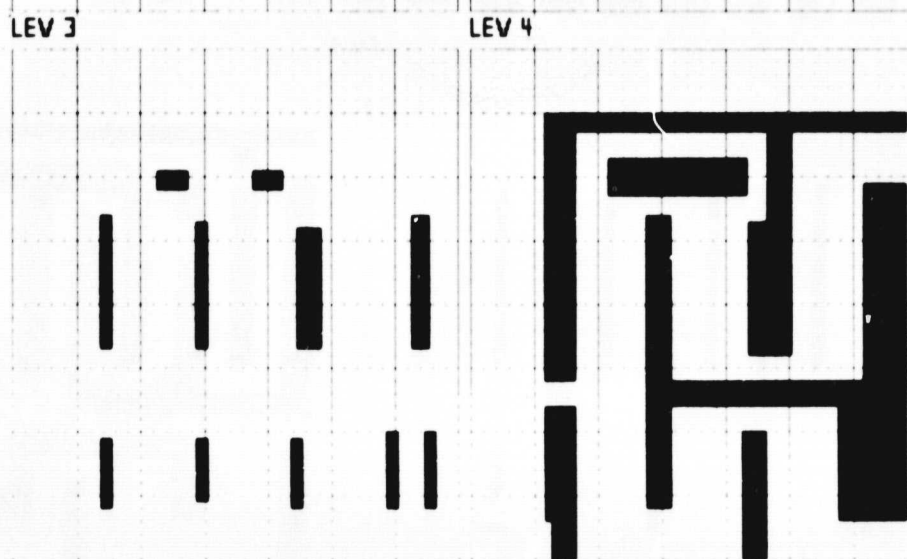
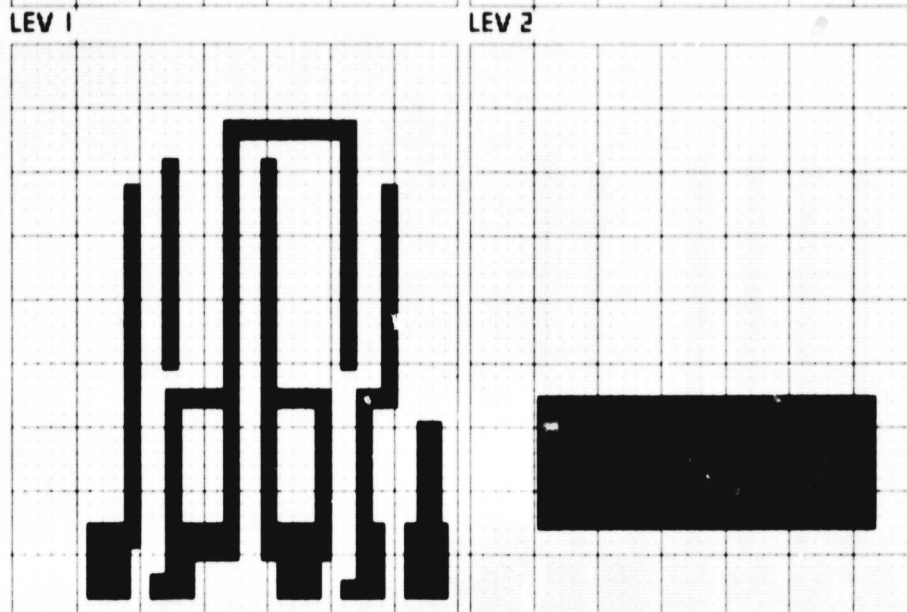
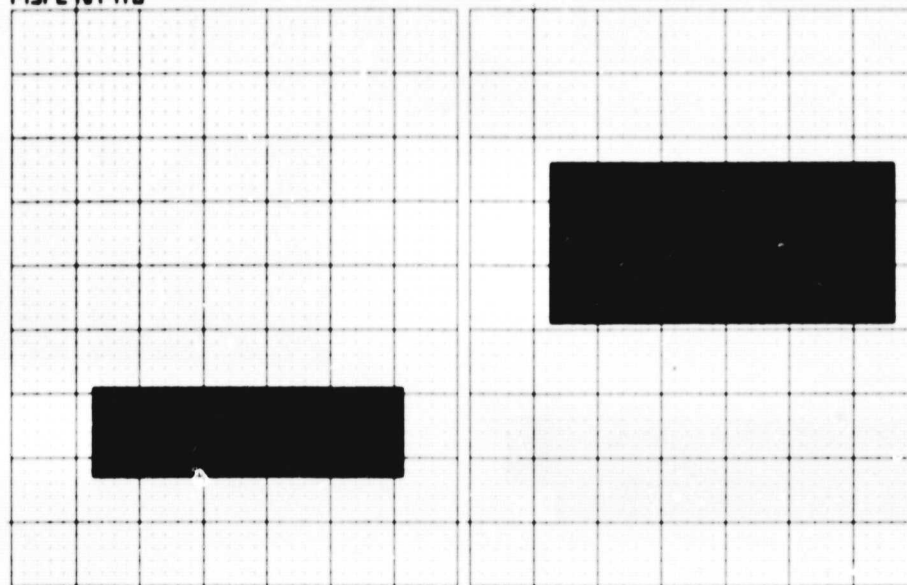


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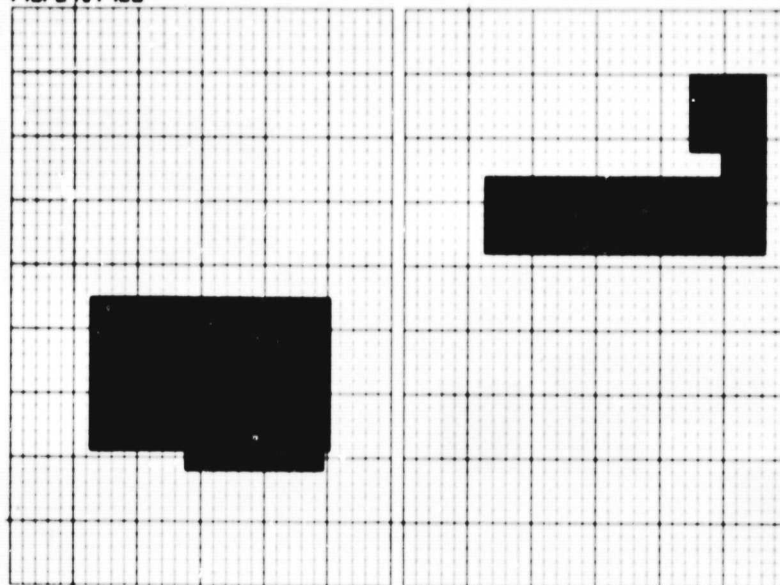


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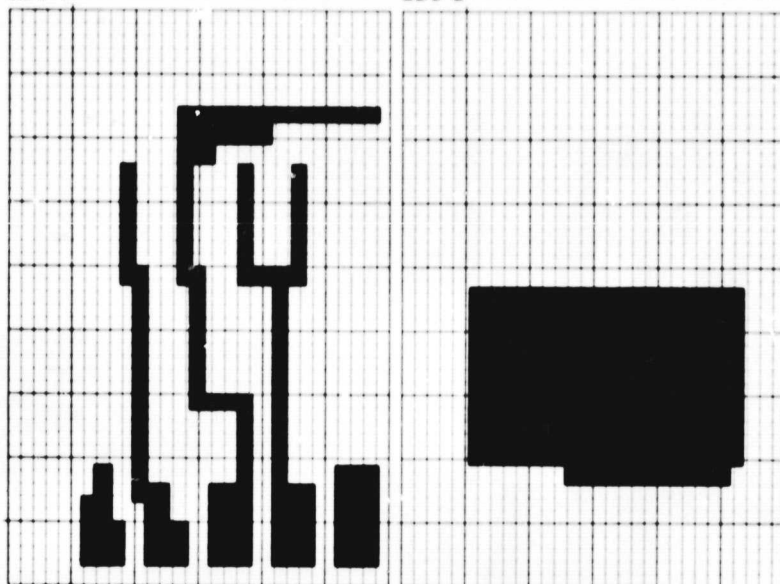
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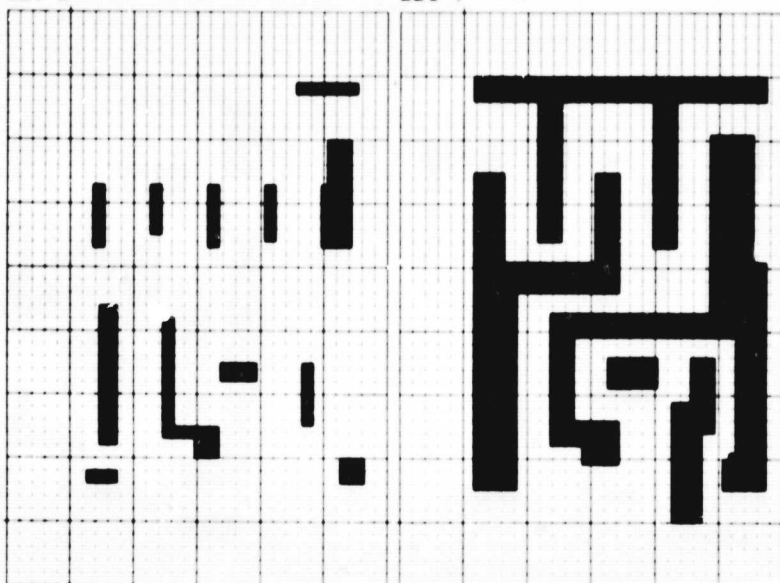
LEV 1

LEV 2



LEV 3

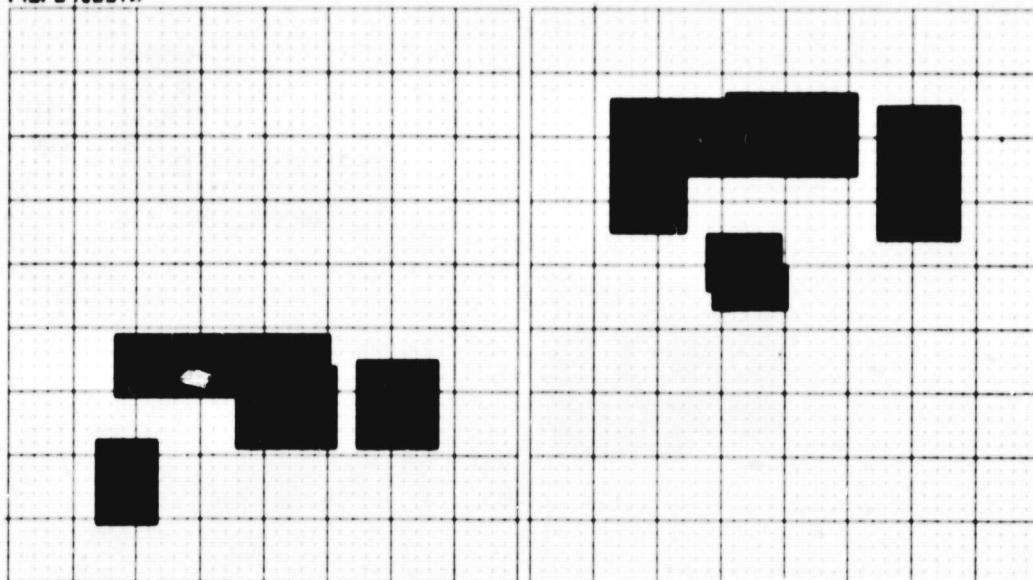
LEV 4



LEV 5

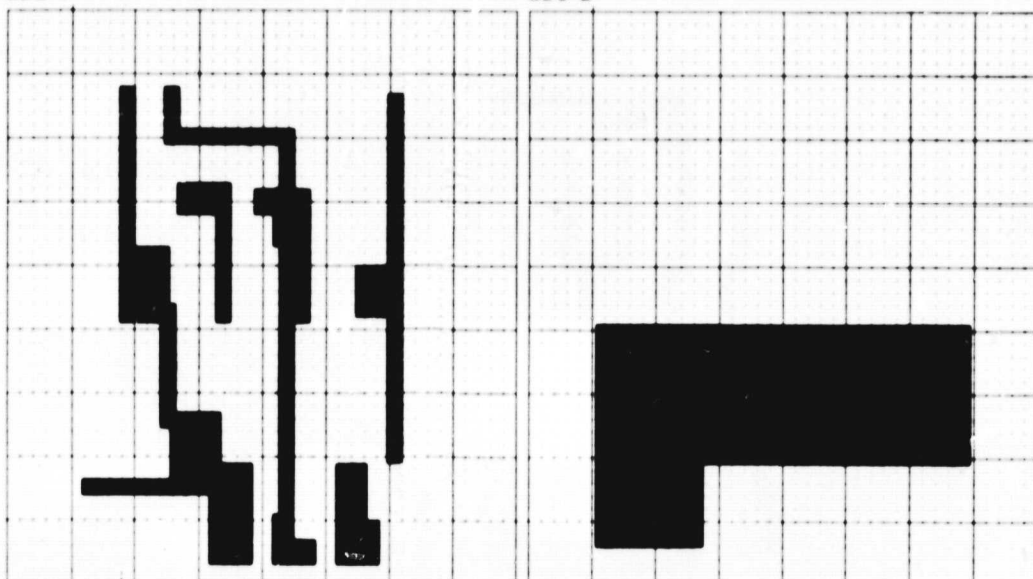
17 LEV 6

MSFC N2310



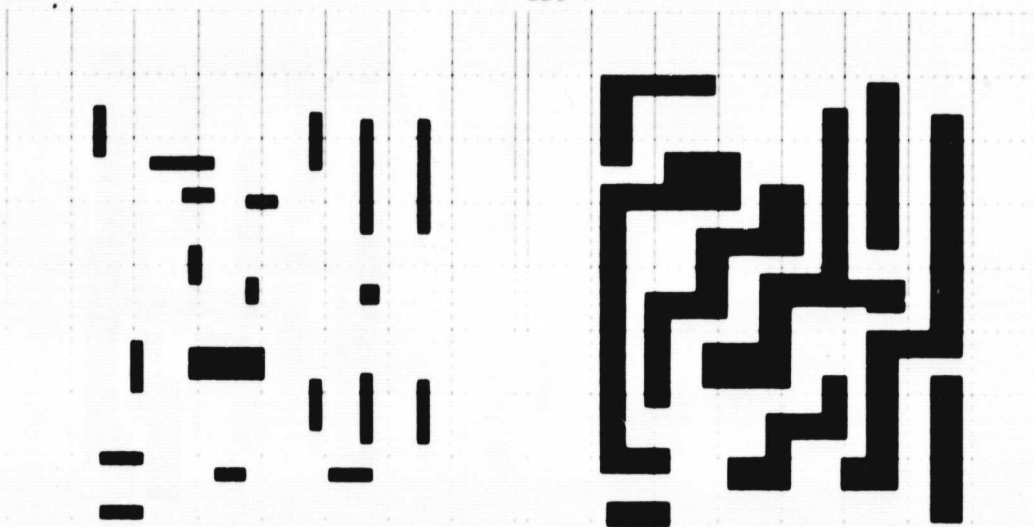
LEV 1

LEV 2



LEV 3

LEV 4

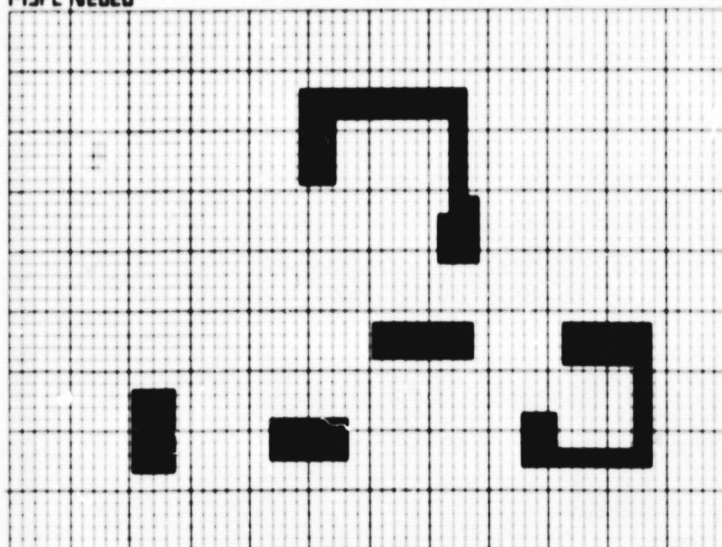


LEV 5

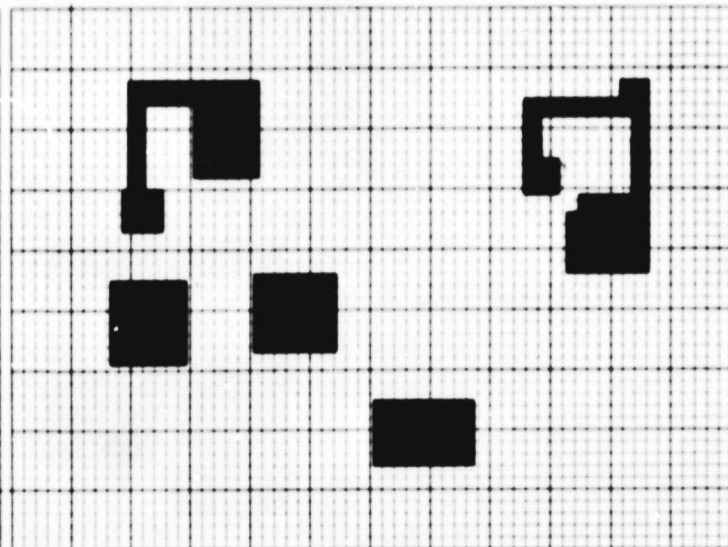
18 LEV 6

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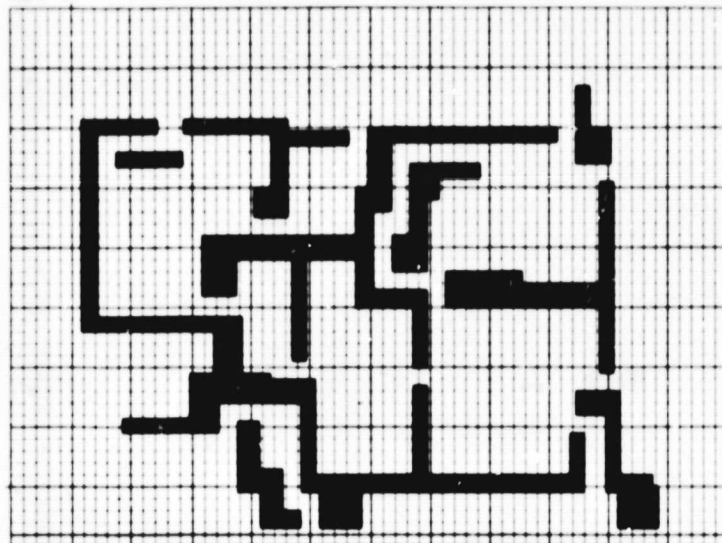
MSFC N2020



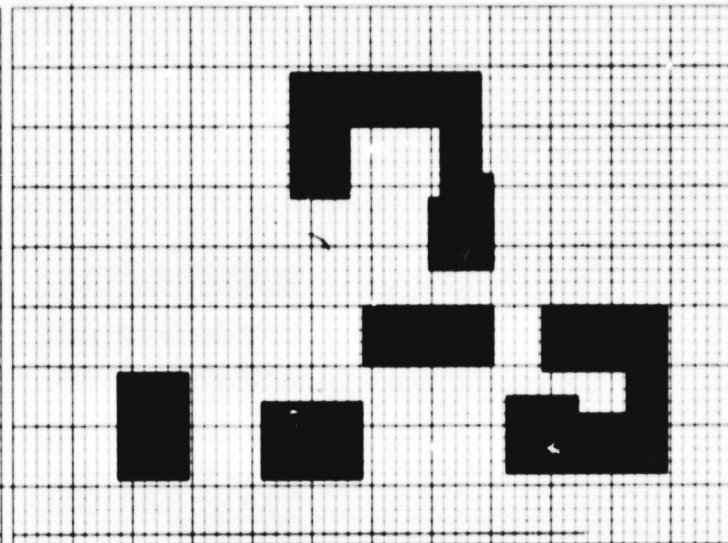
LEV 1



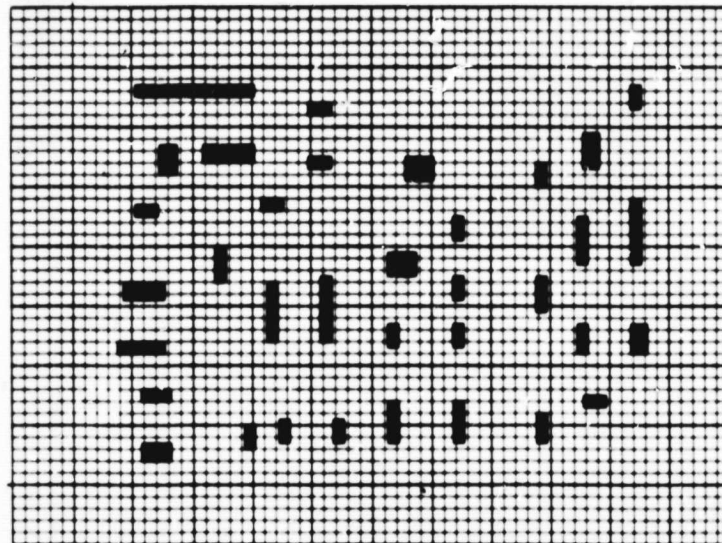
LEV 2



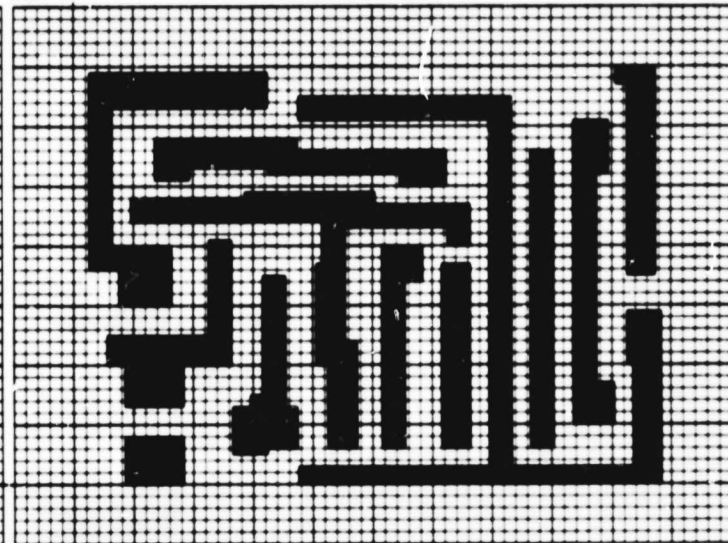
LEV 3



LEV 4

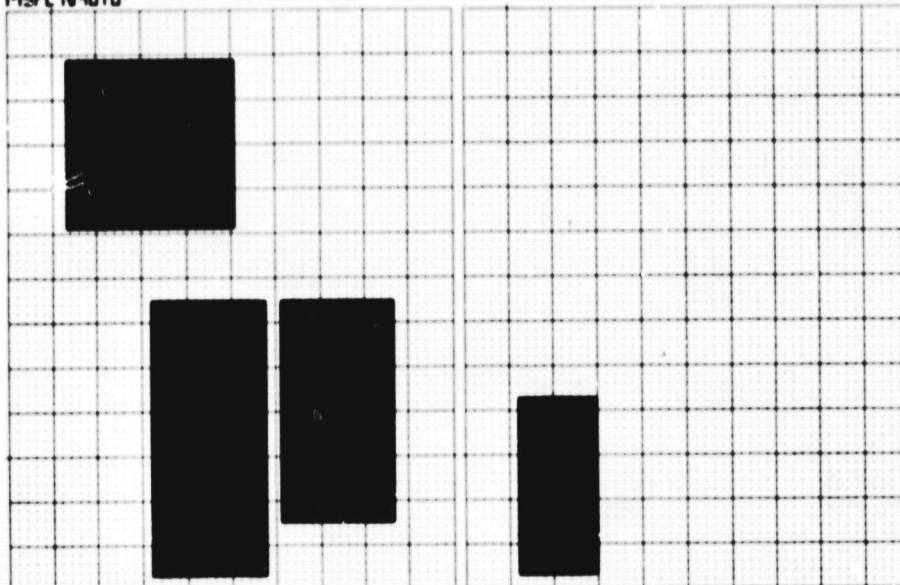


LEV 5



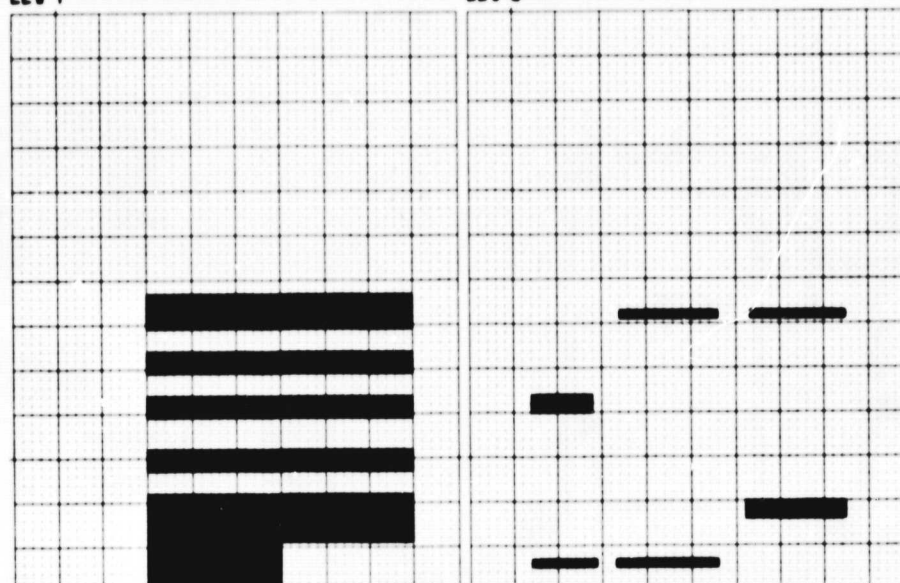
LEV 6

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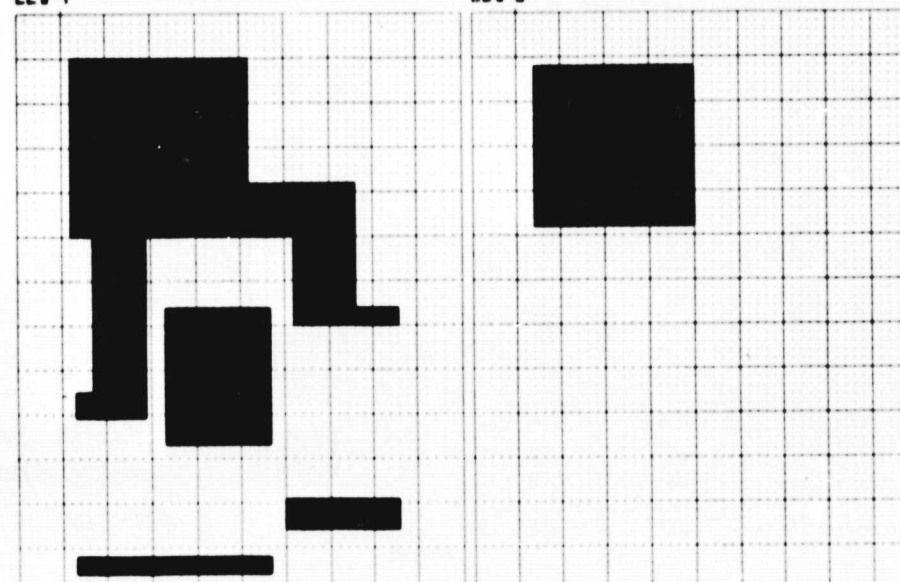
LEV 1

LEV 3



LEV 4

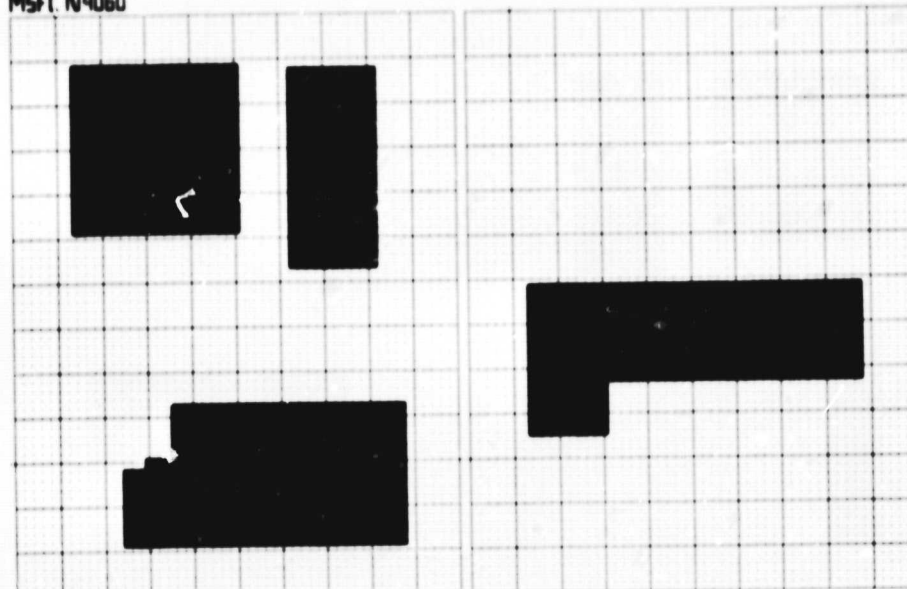
LEV 5



LEV 6

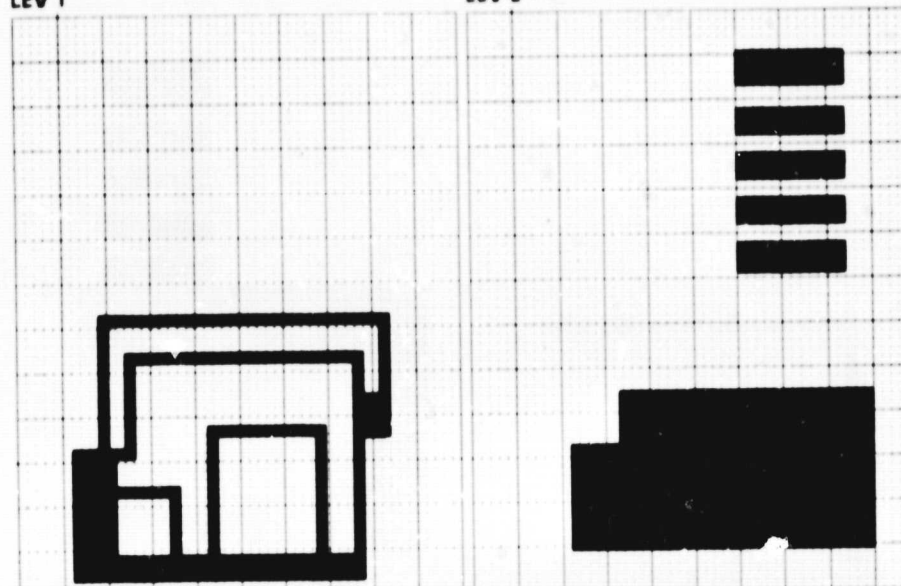
20 LEV 7

MSFC N90b0



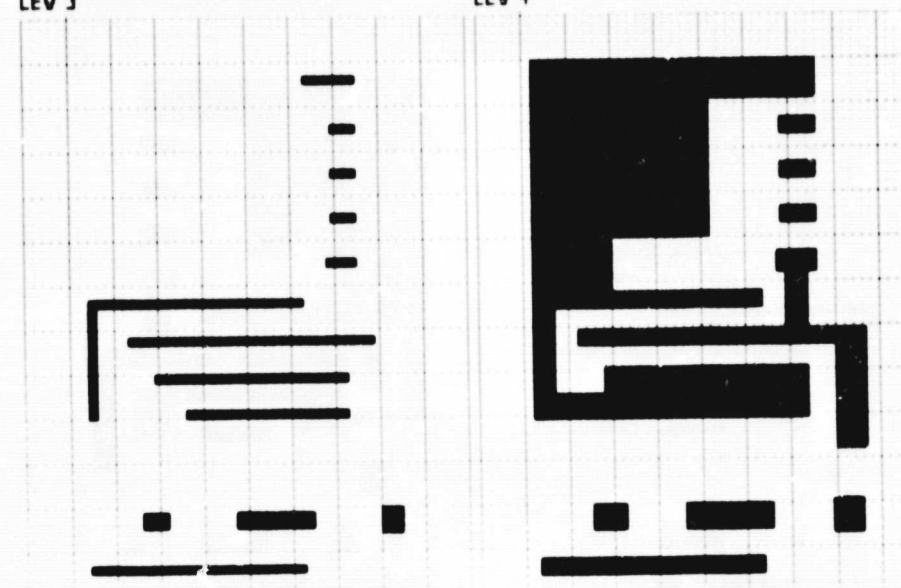
LEV 1

LEV 2



LEV 3

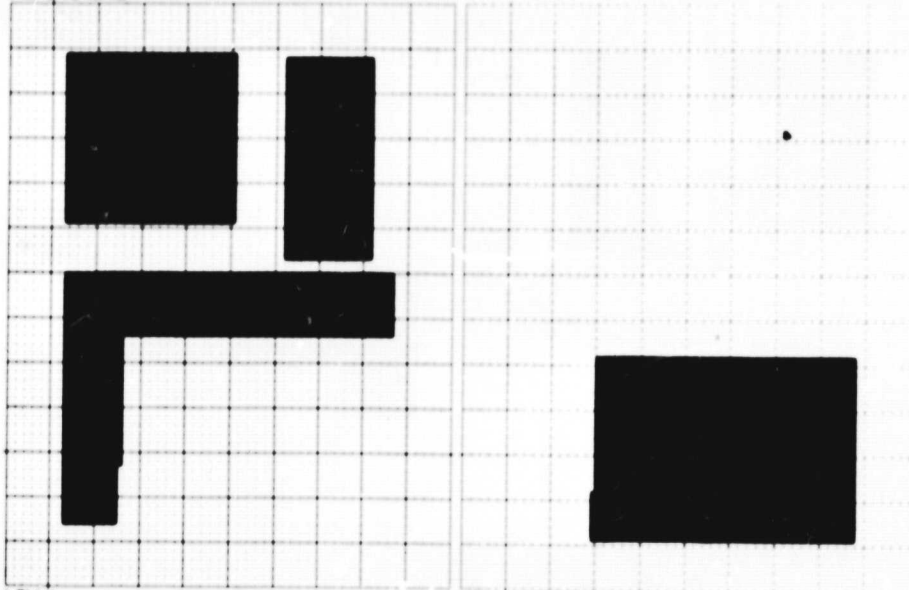
LEV 4



LEV 5

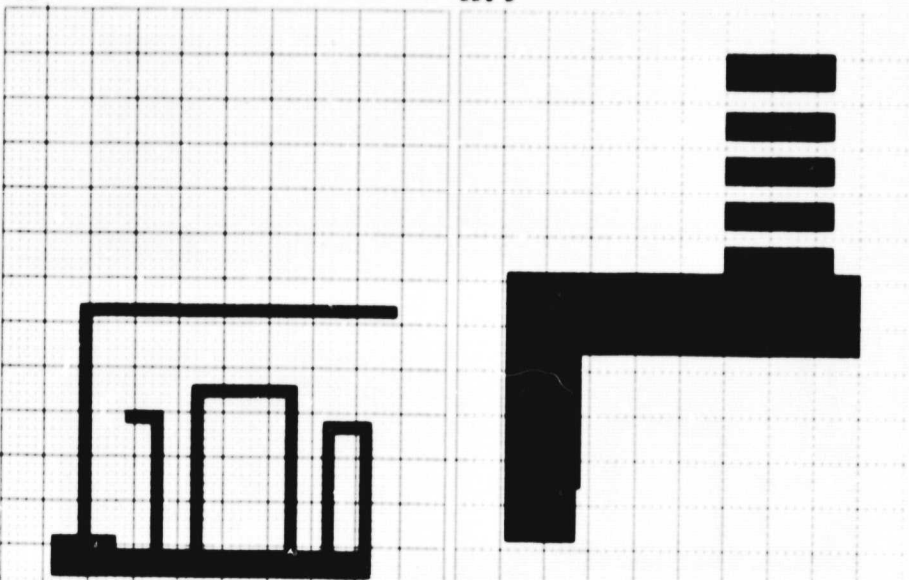
21 LEV 6

M5FC N9070



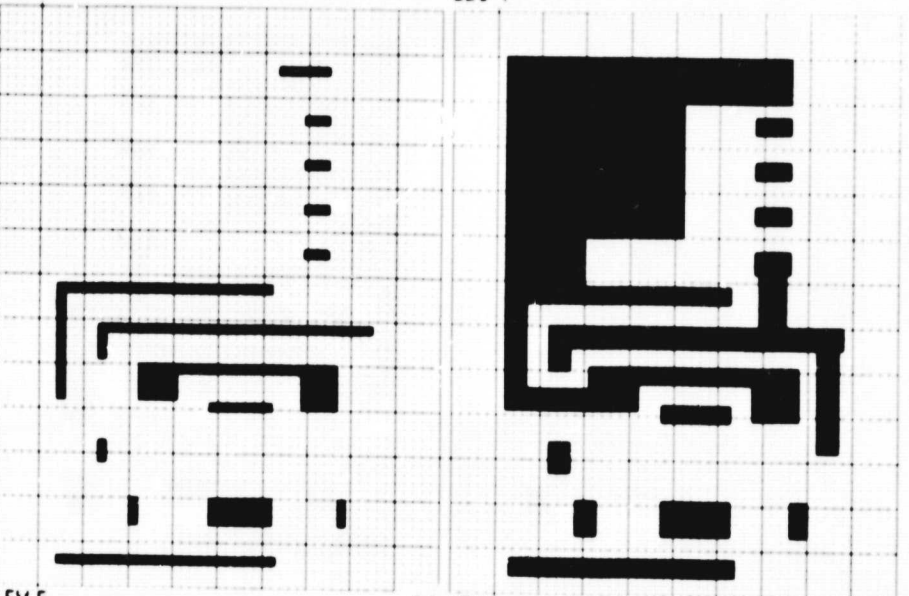
LEV 1

LEV 2



LEV 3

LEV 4

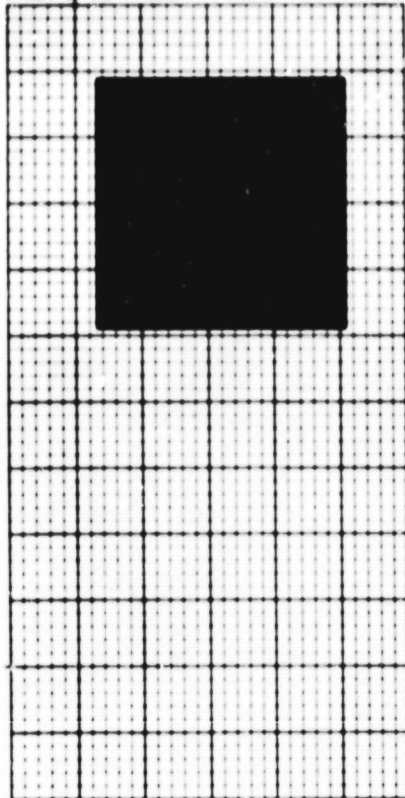


LEV 5

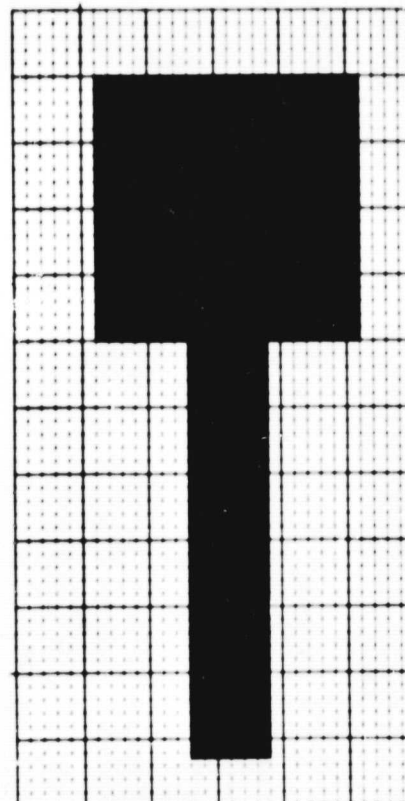
22 LEV 6

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MSFC N9100

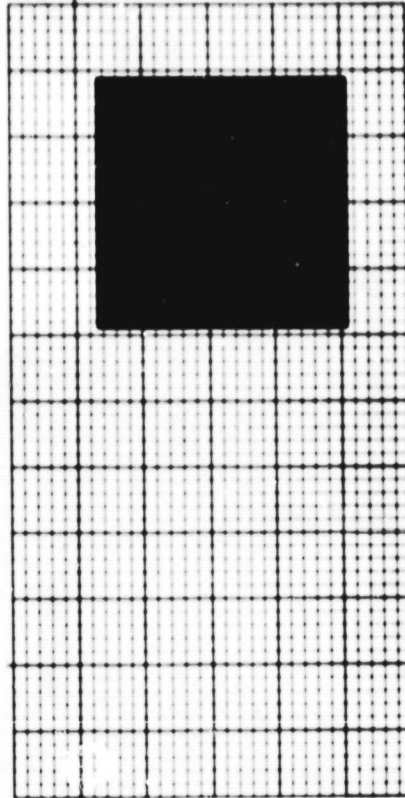


LEV I

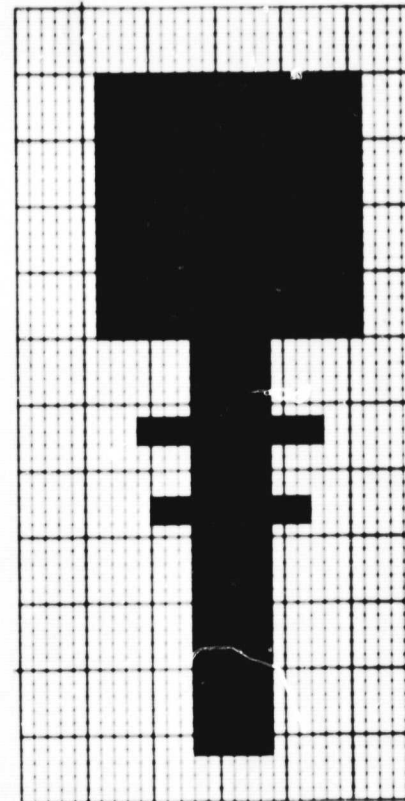


LEV b

MSFC N9110

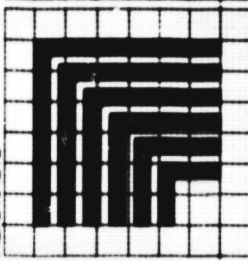


LEV I

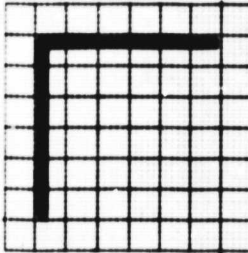


LEV b

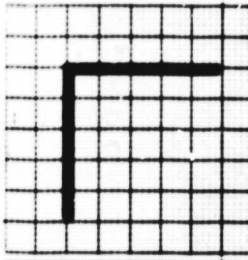
POST INDEX



LEV 1

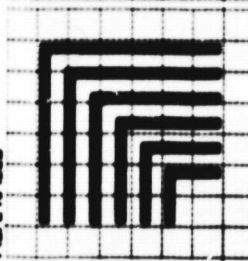


LEV 2

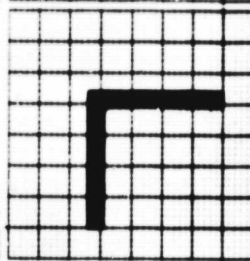


LEV 3

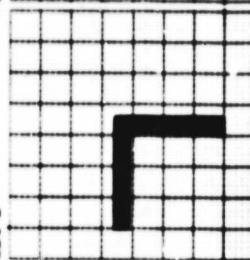
POST INDEX



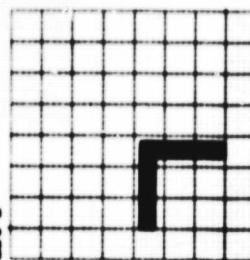
LEV 1



LEV 4

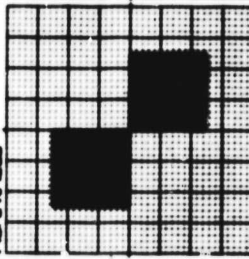


LEV 5



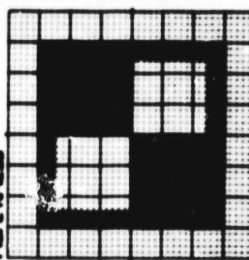
LEV 6

POST INDEX



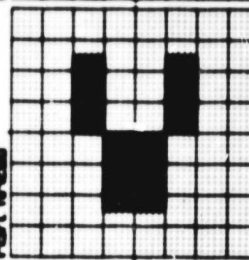
LEV 1

POST INDEX



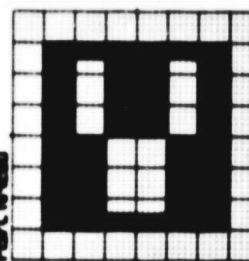
LEV 3

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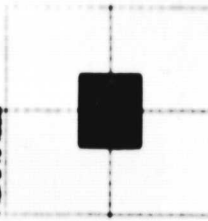
LEV 1

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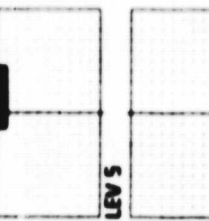
LEV 3

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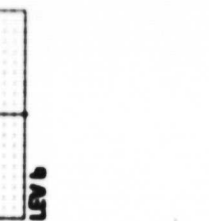
LEV 1

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LEV 5

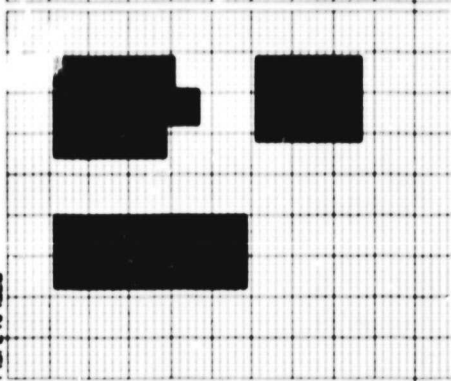
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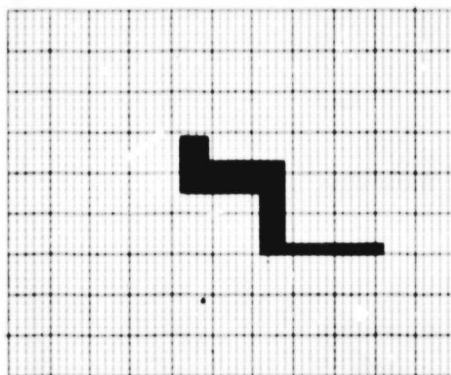
LEV 6

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MSFC N9320

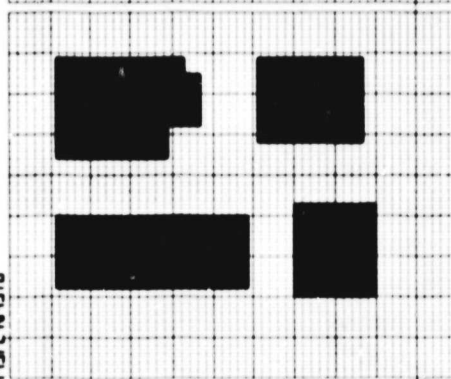


LEV 2

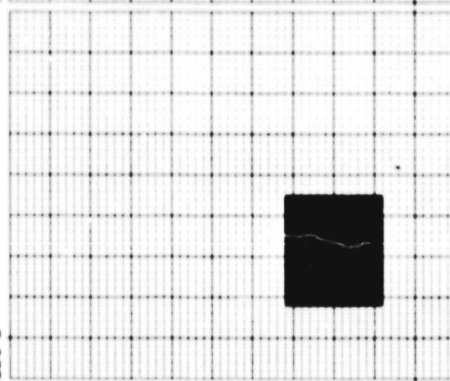


LEV 3

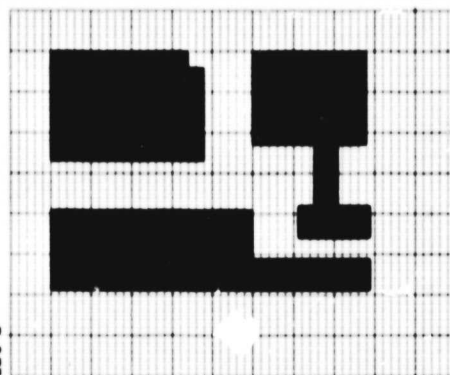
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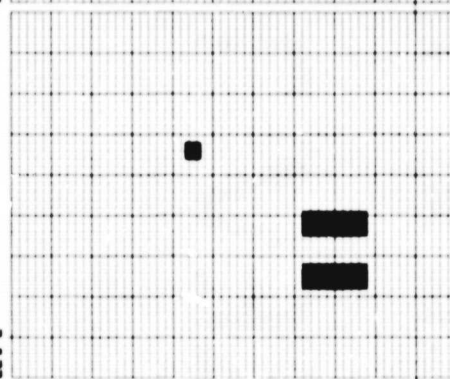
LEV 2



LEV 4

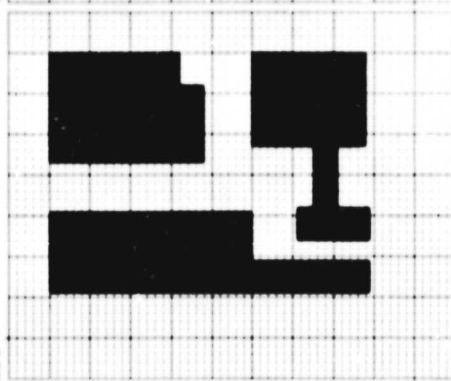


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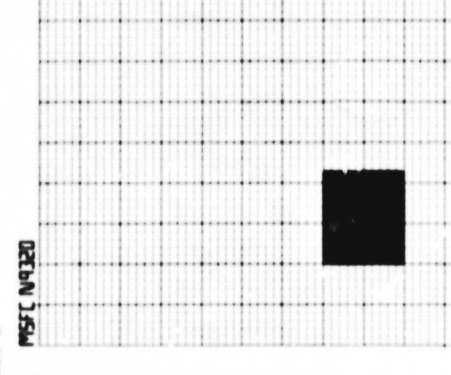


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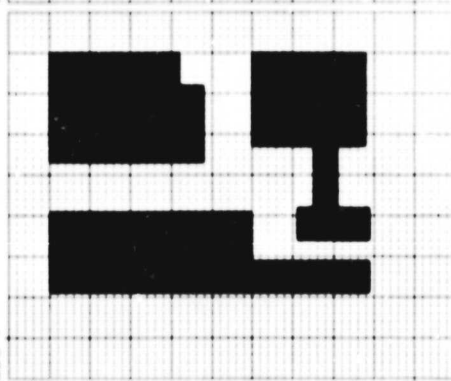
LEV 5



LEV 6



LEV 1



LEV 7

MSFC N9400

LEV 1

LEV 2

LEV 3

MSFC N9700

LEV 1

MSFC N9710

LEV 1

MSFC N9720

LEV 1

LEV 4

LEV 5

LEV 6

MSFC N9750

MSFC N9740

MSFC N9730

LEV 7

LEV 8

LEV 9

MSFC N9780

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MSFC N9760

MSFC N9410

LEV 1

MSFC N9420

LEV 1

MSFC N9440

LEV 9

MSFC N9450

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MSFC N9470

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MSFC N9480

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MSFC N9490

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